



# Pharos

## Monolithic 12-Port ADSL CO PHY

### Overview

The Pharos CT-L48SC12 CO chipset is a complete, high-performance, 12-port solution for low-power, high-density, ATU-C line card applications.

Pharos is a sixth generation Centillium Communications ADSL CO chipset that builds upon many years of ADSL deployment experience. With its low power and extensive feature set, it is the ideal engine for advanced, state-of-the-art line cards for DSLAM, MTU/MDU, DLC, and MSAP equipment.

The Pharos CO chipset incorporates multiple interfaces and the eXtremeDSL<sup>Max</sup>™ technology, thus making it the solution of choice for high-speed, multi-service line card platforms catering to derived voice and video services applications.

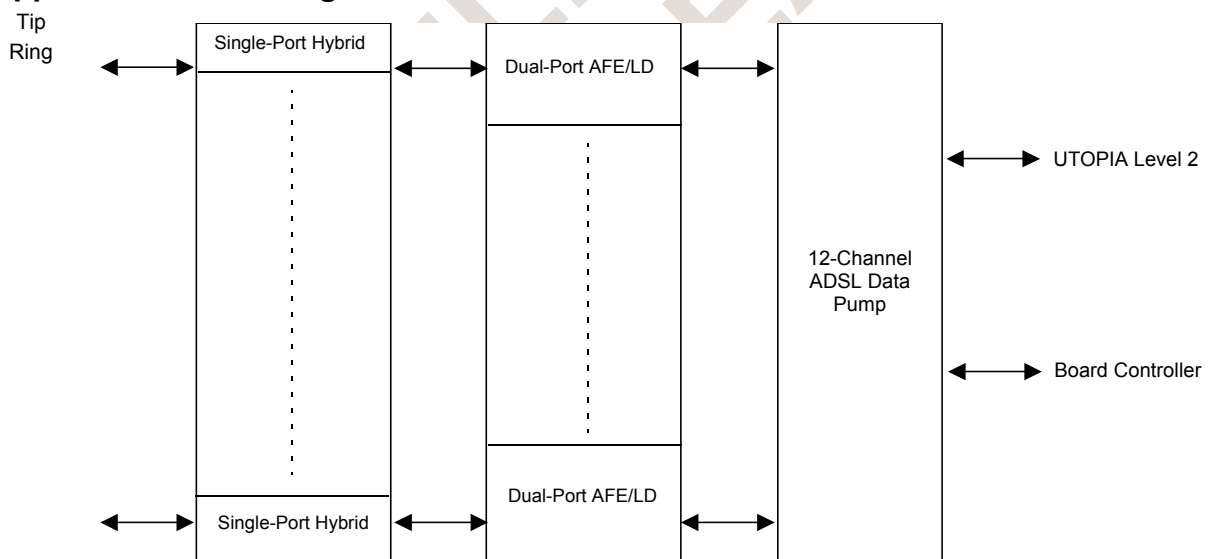
Consisting of a single monolithic 12-port digital processor and a single monolithic two-port AFE (analog front-end), the Pharos chipset provides a low chip-count solution for high-density line cards.

The CT-L48DC12 digital processor provides programmability and high-performance for long-lasting line card solutions.

The CT-L56AC02 AFE chip is a highly integrated device that significantly reduces the requirements on external components, resulting in a reduced system bill of materials.

The high-resolution analog-to-digital and digital-to-analog converter circuits that reside on this AFE chip provide the performance required for high data rate applications.

### Application Block Diagram



## Features

- Highly optimized 12-port, multi-mode ADSL, ADSL2, ADSL2+ (also known as ADSL2plus), and ADSL2++ (also known as quad-spectrum mode)
- Fully supports ADSL2 training/framing (ADSL2 feature set is backwards compatible with ADSL)
- Compliance with the following ITU-T specifications:
  - ITU-T G.992.1 (ADSL G.dmt), with associated annexes
  - ITU-T G.992.2 (ADSL G.lite) with associated annexes
  - ITU-T G.992.3 (ADSL2) with focus on ADSL over POTS, and ADSL over ISDN
  - ITU-T G.992.5 (ADSL2+) with associated annexes
  - ITU-T G.994 (G.hs)
  - ITU-T G.997.1 (G.ploam)
- High-performance ADSL engine supports the following loop profiles:
  - ADSL2+ peak rates of 1.3 Mbps upstream and supporting 25 Mbps downstream for short/medium loops with high-bit loading capability
  - ADSL2 peak rate of 3 Mbps with support for extended upstream, Annex M
  - Long reach ADSL2 that supports 128 kbps symmetrical up to 18 kft
  - ADSL2++ peak rates of 6 Mbps upstream while supporting 50 Mbps downstream for short/medium loops with high-bit loading capability
- Ultra low-power chipset solution with integrated line driver that is based on state-of-the-art process geometry
- LA-PM (loop adaptive power management) scheme that adjusts power consumption with the loop characteristics
- IN-SS (intelligent spectrum selection) algorithm that optimally switches the PSD mask based upon the loop profile
- LA-IM (loop adaptive impedance matching) scheme that optimizes performance at the presence of bridge taps
- LA-SRA (loop adaptive seamless rate adaptation) that dynamically maintains link integrity despite changing noise conditions in the loop
- IN-LM (intelligent link management) feature suite that assists service providers in automating fault detection and the recovery aspect of OM (operation and maintenance)
- Low component count for CO hybrid based on high level of front-end integration for Annex A/B combination line cards
- Supports IN-MCP (intelligent multi-channel payload) that enables simultaneous transport of different traffic types (dual-latency)
- Programmable meter tone filters (both 12 KHz and 16 KHz) for the European markets
- Supports TC-ATM layer UTOPIA Level 2 with 16-bit, up to 50 MHz speed
- Supports the eXtremeDSL<sup>Max</sup>™ technology and feature set for high data rate and long reach
- Less than 1 square inch per port of PCB area (from UTOPIA to tip and ring)
- No external memory required
- Per channel feature provisioning capability
- Hardware support
  - Echo cancellation capability for optional spectrum overlap operation
  - 8-bit or 16-bit UTOPIA Level 2 bus
  - Viterbi on upstream
  - Transmit widening
  - ATM cell header compression
- High-performance modes
  - Single-spectrum (ADSL)
  - Double-spectrum (ADSL2+)
  - Quad-spectrum (ADSL2++)
  - Trellis coding and Viterbi
- 16-bit host interface
  - Muxed data and address mode
  - Non-muxed data and address mode
- -40°C to 85°C operation
- In-band control and monitoring by using the UTOPIA Level 2 bus

## Part Ordering Information


**CT-L48DC12 Digital Processor**

- 12-port ADSL DSP chip
- Single, low-cost external crystal operation
- Programmable core for software upgrades
- No external memory required (on-chip interleaver)
- UTOPIA Level 2, 50 MHz interface for ATM data transfer
- Glueless interface to various host processors
- Extended UTOPIA addressing supports up to 255 PHYs without any additional external logic
- JTAG (IEEE 1149.1) boundary scan
- 16-bit host interface
- Muxed and non-muxed address modes
- Per channel operation of all features

**Analog Front End/Line Driver**

- Two-port, high-resolution, low-power AFE and line driver
- Complete AFE for ADSL CO line cards
- Low-power  $\pm 12V$  line driver
- Extended upstream spectrum (G.992.5 Annex M)
- Single 3.3V supply with on-chip regulator for 1.8V logic supply and charge pump for 5.25V LNA (low noise amplifier) supply
- Receive programmable gain from 0 dbm to 30 dbm in 1.5 dbm steps
- Integrated Annex B and billing tone high-pass filter
- Low-noise pre-amplifier with programmable gain from -6 dbm to 9 dBm in 3 dBm steps
- Digital interface at 35.328 MHz on two wires (double data rate mode for ADSL2++)

**Part Ordering Information**

Product	Chipset	Function	Part Number	Package
Pharos (ADSL2, ADSL2+, and ADSL2++)	CT-L48SC12	Digital Chip	CT-L48DC12-PM	456-pin PBGA
		Analog Chip	CT-L56AC02-QA	108-pin QFN
 <b>Note</b> The chipset must be ordered in sets. Orders of individual components are filled as chipset orders.				



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