Colt CE 100 System on Chip (SoC)

- IEEE 802.1d Bridge
- PON (passive optical network) SerDes and CDR (clock and data recovery)
- 256-Kbytes Program RAM
- MIPS 4Kc® CPU core
- Wirespeed Encryption Block

the edge in broadband™

The Colt™ 100 SoC supports the complex set of capabilities required by service providers deploying Central Office equipment (CO) in Ethernet Passive Optical Networks. In association with Centillium's complementary CPE chip, the Mustang™ 200, Colt supports all the protocol requirements and relevant standards applicable to a highly efficient, cost effective roll out of an EPON infrastructure.

High Level Hardware and Software Integration

The Colt 100 is a highly integrated, cost effective, mixed-signal EPON protocol processing solution that is fully compliant with IEEE 802.3ah. The Colt 100 integrates the following components into a complete single-chip solution for EPON OLT deployment:

- IEEE 802.1d bridge
- PON (passive optical network) SerDes and CDR (clock and data recovery)
- GMII (Gigabit media independent interface), WAN interface (wide area network interface)
- CAM (content addressable memory)
  - 256-Kbytes boot RAM
- MIPS 4Kc® CPU core

The Colt 100 resides on a line card at a service provider central office and directs traffic to multiple ONUs (optical network units). It supports P2PE (point-to-point emulation) as specified in IEEE 802.3ah using MPCP (multi-point control protocol) and also supports multiple MAC clients using SCB (single copy broadcast). Interconnection between the WAN (wide area network) and the Colt 100 can be achieved via either standard copper or fiber interfaces.

Support for the MIPS RISC core is enabled by an external host CPU. A fully featured software package is provided with the Colt 100. This complete software subsystem contains the instruction set for the inbuilt core, including the highly efficient DBA, and control and API support for the host CPU. The systems developer is presented with a total offering allowing very fast integration of the OLT with minimization of software development effort, and a flexible framework for feature development.

Integrated Bridging

The Colt 100 bridge complies with IEEE 802.1d. Its VLAN (virtual local area network) processing capabilities comply with IEEE 802.1q. IGMP snooping is supported, enabling management of up to 512 multicast traffic flows.

Efficient Bandwidth Control and Utilization

The Colt 100 DBA (dynamic bandwidth allocation) architecture incorporates a hardware-assisted accelerator as well as firmware running on the integrated MIPS CPU core. As a result, the device achieves a short cycle time without sacrificing overall system efficiency, and supports low-latency traffic. The Colt 100 provides flexible downstream bandwidth control allowing service providers to manage multiple SLAs (service level agreements).

Encryption and Security

Traffic in the downstream direction is encrypted at wirespeed - 1.25 Gbps in EPON mode - using the AES-128 encryption method. Key exchange handshake is supported and on-the-fly encryption key change is possible with no loss of frame. The Colt 100 supports multiple authentication schemes, including IEEE 802.1x, MAC address, and password-based authentication.

The Colt 100 fully complies with IEEE 802.3ah clause 57 OAM (operations, administration and maintenance) and supports mechanisms for monitoring link operations, such as remote-fault indication and remote loop-back control. Remote ONU configuration and monitoring is supported by OAM messages from the Colt 100.

CENTILLIUM COMMUNICATIONS

Colt CE 100 System on Chip (SoC)

Features
- Full compliance with the latest EFM (Ethernet in the first mile) specification, IEEE 802.3ah, including clauses 64 and 65
- Single-chip, mixed-signal solution for OLT applications integrates these components:
  - —Bridge
  - —EPON protocol processor
  - —Burst mode CDR/SerDes for PON interface
  - —CDR/SerDes for the WAN interface
  - —CAM
  - —MIPS CPU core

WAN Interface
- Support for 100Base-TX/1000Base-T (MII/GMII)
- Support for 1000Base-LX/SX with integrated PCS (physical coding sublayer)
- Support for IEEE 802.3x flow control with Pause messages, including a configurable buffer threshold

Bridge
- IEEE 802.1d Layer-2 compliant
- Supports up to 256 logical links
- Configurable ONU-to-ONU communications
- Integrated CAM enables learning of up to 8,192 MAC addresses
- Supports 256 Mbytes of external frame buffering in both directions
- Fully configurable VLAN support based on IEEE 802.1p and 802.1q including removal, addition, forwarding, and learning
- Fully configurable VLAN tag overwrite support
- Support of up to four or eight priority queues in each direction for each logical link based on VLAN tag or IP TOS (type of service)
- IPv4 IGMPv1 and v2 snooping for multicast traffic management
- IPv6 MLD (multicast listener discovery) support

EPON Protocol
- Fully IEEE 802.3ah compliant
- P2PE between each ONU and OLT using an LLID (logical link identifier)
- Support for 256 registered LLIDs
- SCB support
- Complete processing and generation of EFM specified MPCP messages
- Standard discovery and registration, in two proprietary modes:
  - —Explicit serial number
  - —Explicit LLID
- Support for logical link lengths of up to 60 km

Dynamic Bandwidth Allocation (DBA)

DBA with short allocation cycle time and high-bandwidth efficiency includes:
- Hardware-assisted accelerator for REPORT processing and GATE generation
- Algorithm processing using integrated MIPS core
- Low-latency traffic support
- Complete management element statistic collection support
- Multiple DBA algorithms supported through remote firmware download

Scheduler

Downstream scheduler with efficient bandwidth control supports multiple SLAs and low-latency traffic, such as voice.

Encryption
- Supports configurable upstream and downstream encryption based on AES-128, as described in FIPS Publication 197
- Wirespeed (1.25 Gbps) encryption and decryption
- Separate encryption key for each logical link
- Encryption key handshake
- Key change on the fly with no loss of frame
- Separate encryption and decryption keys

Authentication
- Multiple authentication schemes including
  - —IEEE 802.1x
  - —MAC address
  - —Password-based authentication supported
- Authentication per logical link

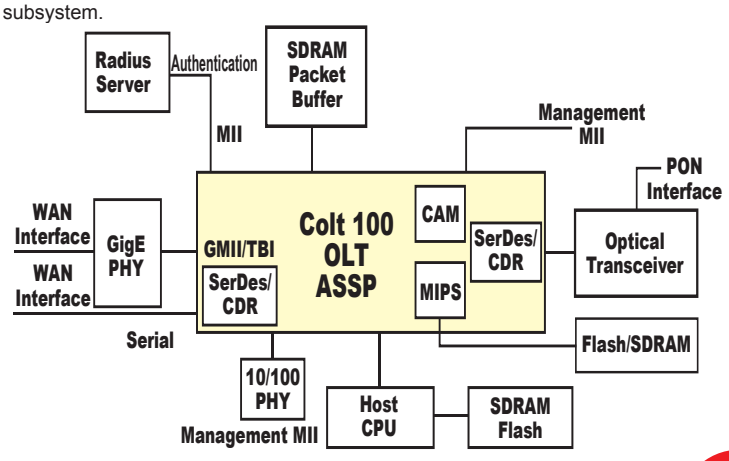
PMD
- Integrated burst mode SerDes/CDR with short sync time for PON interface
- Integrated SerDes/CDR for WAN optical interface
- Multi-vendor PON transceiver interoperability. Interfaces directly to Centillium's Zeus family of transceiver chips.

Management
- Full compliance to IEEE 802.3ah clause 57
- IEEE 802.3/802.3ah Annex 30A management elements support
- Additional proprietary management elements
- Bridge and Ethernet MIB (management information base) support per IETF RFC-1493 and RFC-2674
- Remote ONU management support including:
  - —Alarm detection
  - —ONU configuration and monitoring
  - —Pattern generator and detector for loop test
  - —Shut-down control
  - —Remote Software download (with Mustang 200)
- In-band signaling through the WAN interface and separate MII (media independent interface) for management signaling
- IEEE 802.3x clause 31 port-based flow control with Pause message support

Supported Interfaces
- 32/64-bit SDRAM interface
- WAN side TBI (ten-bit interface)
- WAN side GMII/MII (Gigabit media independent interface/media independent interface)
- PON side TBI
- PON side serial differential interface
- Authentication MII
- Management MII
- MDIO interface to PHY device
- 32-bit Host bus
- 16-bit asynchronous management bus
- FLASH/SRAM
- GPIO (general-purpose input/output) and LED
- Two-wire and SPI (serial peripheral interface)
- JTAG

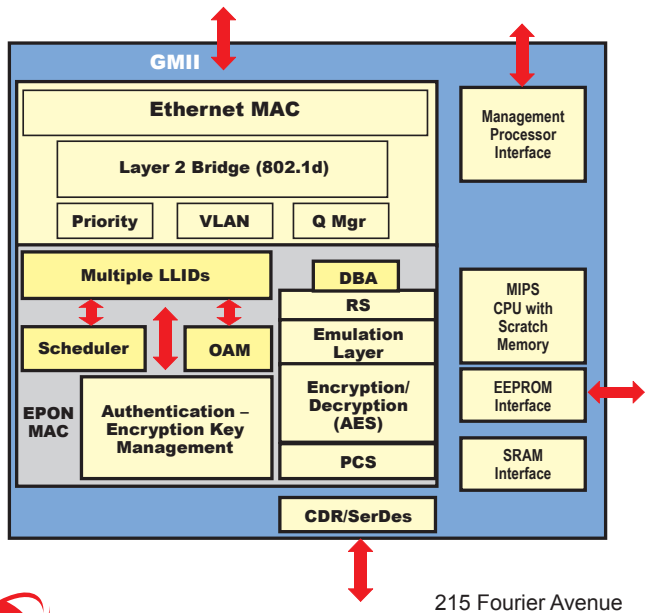
Application Block Diagram

The systems block diagram illustrates the Colt 100 connected to an optical transceiver. The Colt 100 operates with any 802.3ah compliant transceiver subsystem.



Internal System Block Diagram

Illustrating the relationship between the significant internal blocks of the Colt 100 and the major external interfaces:



Part Ordering Information

Product	Function	Part Number	Package
Colt	EPON OLT	CT-TPSMTO2	676-HSBGA

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